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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/330,743	06/11/1999	BRIAN BUCHANAN	RA998-040	9782
25299	7590	11/24/2003	EXAMINER	
IBM CORPORATION PO BOX 12195 DEPT 9CCA, BLDG 002 RESEARCH TRIANGLE PARK, NC 27709			WAXMAN, ANDREW	
			ART UNIT	PAPER NUMBER
			2667	

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/330,743	BUCHANAN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Andrew M Waxman	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 11 October 2003.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 11-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 11-25 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. §§ 119 and 120

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) The translation of the foreign language provisional application has been received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

#### Attachment(s)

- |  |  |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                    | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)           | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . | 6) <input type="checkbox"/> Other: _____ .                                   |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 11, 13 – 16, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartley et al. (US 5,034,908) in view of Berlekamp (US 4,731,676), hereinafter referred to as Hartley and Berlekamp respectively.

Regarding claims 11, 24, and 25, Hartley discloses a device that handles plural lines of data and transfers serial data to parallel bits 18 (Figure 8) and (Figure 12) where a word latch stores in memory a predefined group of bits, where a programmed computer of computation device is inherent to accessing a memory bit storage device and an aligner to handle the inherent misalignment for the predefined bit patterns in a linear fashion (Col 32, lines 33-43) and a memory RAM for the words to be written too (Col 21, lines 65-67).

Hartley does not expressly disclose storing in a computer memory bit patterns representing different groups of parallel bit streams, searching the memory to detect a predefined bit pattern stored in each group, measuring the misalignment between at least 2 groups, and using the misalignment measurement to adjust the bit patterns until the bit patterns are aligned.

Berlekamp discloses storing in a computer memory ('buffer' col. 1 lines 45 - 52) bit patterns representing different groups of parallel bit streams (col. 1 lines 54 – 56), searching the memory to detect a predefined bit pattern stored in each group (col. 4 lines 28 – 36), measuring the misalignment between at least 2 groups (col. 1 lines 60 – 67), and using the misalignment measurement to adjust the bit patterns until the bit patterns are aligned (col. 2 lines 61 – 64). See also col. 2 lines 51 – 64.

Therefore, at the time the invention was made it would have been obvious to one of ordinary skill in the art to include the synchronization method, as disclosed by Berlekamp, into the invention as disclosed by Hartley.

One of ordinary skill in the art would have been motivated to do this in order to reduce the amount of bandwidth consumed by the transmission of synchronization information thereby creating a more efficient communication system. See Berlekamp col. 2 lines 1 – 8.

Regarding claims 13-16, Hartley further discloses a plurality of system operable to receive serial data to generate parallel data 73 and 78 (Figure 17) and a system for generating a plurality of serial streams 80-83 (Figure 18) and having a high speed bus attached (Figure 9) and a data recover circuit operable to handle a nibble of data bits as described above.

***Claim Rejections - 35 USC § 103***

2. Claims 12, and 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartley in view of Berlekamp and further in view of Pocrass (US 5,428,806).

Regarding claims 12 and 17-19, Hartley in view of Berlekamp discloses all of the limitations as recited above with respect to claim 11.

Hartley in view of Berlekamp does not expressly disclose a controller and a bit pattern of 0101.

Pocrass teaches a system of transmitting and receiving with 3-bit latches (figure 6B) and an arrangement with 4 data lines (Col 11, lines 13-16) and the use of memory to store data that had undergone a serial to parallel conversion for bit streams of data word types (Col 9, lines 45-50), where the bit word pattern 0101 is from a list of binary representations for the fourteen slots in the hardware device respectively one being 0101, (Col 19, 34-55) and a controller 142 (Figure 6A) used to control the accessing of memory.

Therefore, at the time the invention was made it would have been obvious to one of ordinary skill in the art to have included the use of a bit pattern, as disclosed by Pocrass, into the invention as disclosed by Hartley in view of Berlekamp.

One of ordinary skill in the art would have been motivated to do this in order to represent the number five as a value associated with an element of the references as five is a small enough value to be included in a table of values counting up to fourteen and to include a controller for easy access to stored data patterns.

***Claim Rejections - 35 USC § 103***

3. Claims 20 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartley et al. (US Patent No. 5034908) in view of Pocrass (US Patent No. 5428806).

Regarding claims 20 – 23, Hartley discloses a system with recovery circuits and an alignment correction with serial and parallel bit streams and a latch for word (Figures 17-25, 26b) and a plurality of multiplexers 30-33 using the latch command (Col 29, lines 5-10) and (Figure 10) where the number of parallel sets of storage devices is four (Figure 10) 34-37 and a memory or storage device delay elements attached to the multiplexers (34-37) (Figure 10) and a plurality of multi-bit latches serially connected, 19 (Figures 11 and 12) 79 (Figure 17) and 94 (Figure 18) and a processor 57 (Figure 13).

Hartley does not expressly disclose a controller and a bit pattern of 0101.

Pocrass discloses a system of transmitting and receiving with 3-bit latches (figure 6B) and an arrangement with 4 data lines (Col 11, lines 13-16) and the use of memory to store data that had undergone a serial to parallel conversion for bit streams of data word types (Col 9, lines 45-50), where the bit word pattern 0101 is from a list of binary representations for the fourteen slots in the hardware device respectively one being 0101, (Col 19, 34-55) and a controller 142 (Figure 6A) used to control the accessing of memory.

Therefore, at the time the invention was made it would have been obvious to one of ordinary skill in the art to have included the use of a bit pattern, as disclosed by Pocrass, into the invention as disclosed by Hartley.

One of ordinary skill in the art would have been motivated to do this in order to represent the number five as a value associated with an element of the references as five is a small enough value to be included in a table of values counting up to fourteen and to include a controller for easy access to stored data patterns.

***Response to Arguments***

Applicant's arguments with respect to claims 11 – 25 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Roberts discloses a telecommunications system with arbitrary alignment parallel framer.

Widmer discloses a serial-to-parallel converter using alternating latches and interleaving techniques.

Bartow discloses frame group transmission and reception for parallel/serial buses.

Aoki discloses a skew compensation circuit effectively operated during readout in a reverse sense.

Loeb discloses an optical fiber system.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

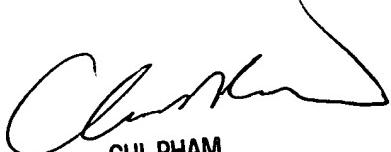
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew M Waxman whose telephone number is (703) 305-8086. The examiner can normally be reached on 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Andrew M. Waxman

  
CHI PHAM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600 n/9/03